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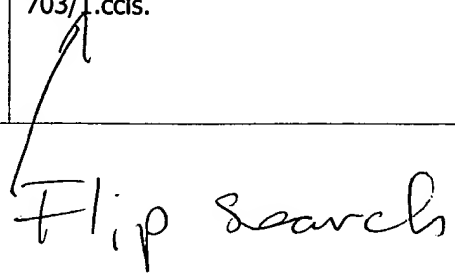

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1 The hierarchical task graph and its use in auto-scheduling

Constantine D. Polychronopoulos

June 1991 **Proceedings of the 5th international conference on Supercomputing**

Full text available: pdf(1.24 MB) Additional Information: full citation, references, citings, index terms

2 MAGELLAN: multiway hardware-software partitioning and scheduling for latency minimization of hierarchical control-dataflow task graphs

Karam S. Chatha, Ranga Vemuri

April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

Full text available: pdf(522.98 KB) Additional Information: full citation, abstract, references, citings, index terms

The paper presents MAGELLAN, a heuristic technique for mapping hierarchical control-dataflow task graph specifications on heterogeneous architecture templates. The architecture can consist of multiple hardware and software processing elements as specified by the user. The objective of the technique is to minimize the worst case latency of the task graph subject to the area constraints on the architecture. The technique uses an iterative approach consisting of closely linked hardware-softwa ...

3 Low level scheduling using the hierarchical task graph

David R. Wallace

August 1992 **Proceedings of the 6th international conference on Supercomputing**

Full text available: pdf(971.67 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces a new efficient instruction scheduling algorithm that can schedule across basic blocks. Scheduling globally, across basic blocks, is done by using an extension of the control flow graph (CFG) that combines both data and control dependence constraints. It organizes control flow into a hierarchy of dags and includes dataflow edges that cross basic blocks. We assume a type of extended CFG called the hierarchical task graph (HTG). Previously, the HTG has been used to descr ...

4 Graph models for reachability analysis of concurrent programs

Mauro Pezzè, Richard N. Taylor, Michal Young

April 1995 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 4 Issue 2

Full text available: pdf(3.00 MB) Additional Information: full citation, abstract, references, citings, index terms

The problem of analyzing concurrent systems has been investigated by many researchers, and several solutions have been proposed. Among the proposed techniques, reachability analysis—systematic enumeration of reachable states in a finite-state model—is attractive because it is conceptually simple and relatively straightforward to automate and can be used in conjunction with model-checking procedures to check for application-specific as well as general properties. This article sho ...

Keywords: Ada tasking, process algebra, static analysis

5 Library support for hierarchical multi-processor tasks

Thomas Rauber, Gudula Rünger

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(132.76 KB) Additional Information: full citation, abstract, references, index terms

The paper considers the modular programming with hierarchically structured multi-processor tasks on top of SPMD tasks for distributed memory machines. The parallel execution requires a corresponding decomposition of the set of processors into a hierarchical group structure onto which the tasks are mapped. This results in a multi-level group SPMD computation model with varying processor group structures. The advantage of this kind of mixed task and data parallelism is a potential to reduce the co ...

Keywords: distributed memory, hierarchical decomposition of processor sets, library support, mixed task and data parallelism, multilevel group SPMD, multiprocessor tasks

6 Adaptive Teamwork Coordination Using Graph Matching over Hierarchical Intentional Structures

Susannah Soon, Adrian Pearce, Max Noble

July 2004 **Proceedings of the Third International Joint Conference on Autonomous Agents and Multiagent Systems - Volume 1**

Full text available: pdf(247.21 KB) Additional Information: full citation, abstract

Many existing teamwork coordination approaches recognise team intention by using communications, and/or by identifying plan execution through observing agent actions. However, problems may arise when such information is unavailable, or when agents are not observable at runtime. This paper presents a new agent coordination strategy, called Rolegraphs, that represents and recognises team intentions without requiring full knowledge of plans, or complete observations. The strategy relies on the role ...

7 Parallel program performance prediction using deterministic task graph analysis

Vikram S. Adve, Mary K. Vernon

February 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 1

Full text available: pdf(576.29 KB) Additional Information: full citation, abstract, references, index terms

In this article, we consider analytical techniques for predicting detailed performance characteristics of a single shared memory parallel program for a particular input. Analytical models for parallel programs have been successful at providing simple qualitative insights and bounds on program scalability, but have been less successful in practice for providing detailed insights and metrics for program performance (leaving these to measurement or simulation). We develop a conceptually simple mode ...

Keywords: Analytical model, deterministic model, parallel program performance prediction, queueing network, shared memory, task graph, task scheduling

8 Microarchitecture support for dynamic scheduling of acyclic task graphs
Carl J. Beckmann, Constantine D. Polychronopoulos
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2
Full text available: pdf(1.08 MB) Additional Information: full citation, references, citings, index terms

9 Hierarchical Scheduling and Allocation of Multirate Systems on Heterogeneous Multiprocessors
Yanbing Li, Wayne Wolf
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Full text available: pdf(760.14 KB) Publisher Site Additional Information: full citation, abstract

This paper describes new algorithms for system-level software synthesis, namely the scheduling and allocation of a set of complex tasks running at multiple rates on a heterogeneous multiprocessor. The tasks may have precedence constraints within them. The multiprocessor may be composed of both programmable and fixed-function processing elements and may have arbitrary interconnect topology. Our hierarchical algorithm takes advantage of the hierarchical structure of the system's task graph to hier ...

Keywords: processor scheduling, hierarchical scheduling, hierarchical allocation, multirate systems, heterogeneous multiprocessors, system-level software synthesis, precedence constraints, fixed-function processing elements, programmable processing elements, arbitrary interconnect topology, task graph, hard real-time constraints, multimedia

10 Extracting task-level parallelism
Milind Girkar, Constantine D. Polychronopoulos
July 1995 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 17 Issue 4
Full text available: pdf(1.92 MB) Additional Information: full citation, abstract, references, index terms, review

Automatic detection of task-level parallelism (also referred to as functional, DAG, unstructured, or thread parallelism) at various levels of program granularity is becoming increasingly important for parallelizing and back-end compilers. Parallelizing compilers detect iteration-level or coarser granularity parallelism which is suitable for parallel computers; detection of parallelism at the statement-or operation-level is essential for most modern microprocessors, includin ...

Keywords: code generation, control and data dependence, parallelizing compilers, synchronization

11 A comparison of set-based and graph-based visualisations of overlapping classification hierarchies
Martin Graham, Jessie B. Kennedy, Chris Hand
May 2000 **Proceedings of the working conference on Advanced visual interfaces**
Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

The visualisation of hierarchical information sets has been a staple of Information

Visualisation since the field came into being in the early 1990's. However, at present, support for visualising the correlations between multiple, overlapping sets of hierarchical information has been lacking. This is despite the realisation that for certain tasks this information is as important as the information that forms the individual hierarchies. In response to this, we have produced two early visuali ...

Keywords: authors kit, conference publications, guides, instructions

12 Dynamic task-based anycasting in mobile ad hoc networks

Prithwish Basu, Wang Ke, Thomas D. C. Little

October 2003 **Mobile Networks and Applications**, Volume 8 Issue 5

Full text available: pdf(518.68 KB) Additional Information: full citation, abstract, references, index terms

Mobile ad hoc networks (MANETs) have received significant attention in the recent past owing to the proliferation in the numbers of tetherless portable devices, and rapid growth in popularity of wireless networking. Most of the MANET research community has remained focused on developing lower layer mechanisms such as channel access and routing for making MANETs operational. However, little focus has been applied on higher layer issues, such as application modeling in dynamic MANET environments. ...

Keywords: anycasting, device/service discovery, distributed application execution, mobile ad hoc networks, task graphs

13 Power and energy: A hierarchical approach for energy efficient application design using heterogeneous embedded systems

Sumit Mohanty, Viktor K. Prasanna

October 2003 **Proceedings of the 2003 international conference on Compilers, architectures and synthesis for embedded systems**

Full text available: pdf(399.12 KB) Additional Information: full citation, abstract, references, index terms

Several features such as reconfiguration, voltage and frequency scaling, low-power operating states, duty-cycling, etc. are exploited for latency and energy efficient application design using heterogeneous embedded systems. However, more choices during application design results in a large design space that must be traversed efficiently. In this paper, we propose a hierarchical methodology that integrates optimization heuristics, high-level performance estimators, and low-level simulators to ena ...

Keywords: design space exploration, energy efficiency, heterogeneous embedded systems, performance estimation

14 Hierarchical multi-agent reinforcement learning

Rajbala Makar, Sridhar Mahadevan, Mohammad Ghavamzadeh

May 2001 **Proceedings of the fifth international conference on Autonomous agents**

Full text available: pdf(278.27 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we investigate the use of hierarchical reinforcement learning to speed up the acquisition of cooperative multi-agent tasks. We extend the MAXQ framework to the multi-agent case. Each agent uses the same MAXQ hierarchy to decompose a task into sub-tasks. Learning is decentralized, with each agent learning three interrelated skills: how to perform subtasks, which order to do them in, and how to coordinate with other agents. Coordination skills among agents are learned by using j ...

15 Hierarchical optimization of optimal path finding for transportation applications
Ning Jing, Yun-Wu Huang, Elke A. Rundensteiner
November 1996 **Proceedings of the fifth international conference on Information and knowledge management**
Full text available: pdf(847.96 KB) Additional Information: full citation, references, citings, index terms

16 Learning to Communicate and Act Using Hierarchical Reinforcement Learning
Mohammad Ghavamzadeh, Sridhar Mahadevan
July 2004 **Proceedings of the Third International Joint Conference on Autonomous Agents and Multiagent Systems - Volume 3**
Full text available: pdf(249.15 KB) Additional Information: full citation, abstract

In this paper, we address the issue of rational communication behavior among autonomous agents. The goal is for agents to learn a policy to optimize the communication needed for proper coordination, given the communication cost. We extend our previously reported cooperative hierarchical reinforcement learning (HRL) algorithm to include communication decisions and propose a new multiagent HRL algorithm, called COM-Cooperative HRL. In this algorithm, we define cooperative subtasks to be those subt ...

17 Navigating hierarchically clustered networks through fisheye and full-zoom methods
Doug Schaffer, Zhengping Zuo, Saul Greenberg, Lyn Bartram, John Dill, Shelli Dubs, Mark Roseman
June 1996 **ACM Transactions on Computer-Human Interaction (TOCHI)**, Volume 3 Issue 2
Full text available: pdf(305.99 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Many information structures are represented as two-dimensional networks (connected graphs) of links and nodes. Because these network tend to be large and quite complex, people often perfer to view part or all of the network at varying levels of detail. Hierarchical clustering provides a framework for viewing the network at different levels of detail by superimposing a hierarchy on it. Nodes are grouped into clusters, and clusters are themselves place into other clusters. Us ...

Keywords: data acquisition, fisheye views, hierarchically clustered graphs, information visualization, supervisory control

18 Performance-constrained hierarchical pipelining for behaviors, loops, and operations
Smita Bakshi, Daniel D. Gajski
January 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 1
Full text available: pdf(192.69 KB) Additional Information: full citation, abstract, references, index terms

Behavioral specifications of DSP systems generally contain a number of nested loops. In order to obtain high date rates for such systems, it is necessary to pipeline the system within the behavior, within the loop bodies, and also within the operations. In order to hierarchically pipeline a performance-constrained system, an important step consists of distributing the performance constraint among the loops in such a manner that the constraint is satisfied and design cost is minimized. This ...

Keywords: DSP (digital signal processing) systems, component selection, hierarchical pipelining, loop pipelining, pipelined systems, scheduling

19 Session 5A: Embedded tutorial: embedded software and systems: Low power system

scheduling and synthesis

Niraj K. Jha

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(168.32 KB) Additional Information: full citation, abstract, references, citings, index terms

Many scheduling techniques have been presented recently which exploit dynamic voltage scaling (DVS) and dynamic power management (DPM) for both uniprocessors and distributed systems, as well as both real-time and non-real-time systems. While such techniques are power-aware and aim at extending battery lifetimes for portable systems, they need to be augmented to make them battery-aware as well. We will survey such power-aware and battery-aware scheduling algorithms. Also, system synthesis algorit ...

20 Efficient scheduling of conditional behaviors for high-level synthesis

Apostolos A. Kountouris, Christophe Wolinski

July 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 3

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, citings, index terms

As hardware designs get increasingly complex and time-to-market constraints get tighter there is strong motivation for high-level synthesis (HLS). HLS must efficiently handle both dataflow-dominated and controlflow-dominated designs as well as designs of a mixed nature. In the past efficient tools for the former type have been developed but so far HLS of conditional behaviors lags behind. To bridge this gap an efficient scheduling heuristic for conditional behaviors is presented. Our heuristic a ...

Keywords: Design automation, conditional behavior, high level synthesis (HLS), scheduling

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Ortiz, G.G.; Alduino, A.; Hains, C.; Bo Lu; Lu, Y.-C.; Wen-Lin Luo; Cheng, J.; Zolper, J.C.; Klem, J.A.; Hafich, M.J.;
Lasers and Electro-Optics Society Annual Meeting, 1995. 8th Annual Meeting Conference Proceedings, Volume 1., IEEE , Volume: 1 , 30-31 Oct. 1995
Pages:191 - 192 vol.1

[Abstract] [PDF Full-Text (156 KB)] IEEE CNF

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Antennas and Propagation Society International Symposium, 1992. AP-S. 199 Digest. Held in Conjuction with: URSI Radio Science Meeting and Nuclear EMP Meeting., IEEE , 18-25 July 1992
Pages:1344 - 1347 vol.3

[Abstract] [PDF Full-Text (216 KB)] IEEE CNF

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48 **Advances in thermoplastic coil encapsulation**
Patterson, J.F.B.;
Electrical Electronics Insulation Conference, 1991. Boston '91 EEIC/ICWA Exposition., Proceedings of the 20th , 7-10 Oct. 1991
Pages:176 - 180

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49 **Considerations in the design of a multi-bandwidth, sensitive, wide dynamic range, wide frequency range EMI receiver**
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Electromagnetic Compatibility, 1990. Symposium Record. 1990 IEEE Internati Symposium on , 21-23 Aug. 1990
Pages:634 - 637

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

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50 **A parallel computing architecture for intelligent sensory data processing**
Graham, J.H.;
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Pages:623 - 627

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

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51 **Applications of knowledge based systems to surveillance**
Vannicola, V.C.; Mineo, J.A.;
Radar Conference, 1988., Proceedings of the 1988 IEEE National , 20-21 April

Pages:157 - 164

[Abstract] [PDF Full-Text (504 KB)] **IEEE CNF**

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52 **The effectiveness of monostatic and bistatic deployment of low frequency active sonar**
Mountain, J.A.R.; Ainslie, M.A.; Martin, P.L.R.; Hughes, M.R.; Seto, L.Y.; Lake R.A.; Robins, A.J.;
Multifunction Radar and Sonar Sensor Management Techniques (Ref. No. 2001/173), IEE , 26 Nov. 2001
Pages:11/1 - 11/8

[Abstract] [PDF Full-Text (353 KB)] **IEE CNF**

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53 **STAP for circular forward looking array antennas**
Klemm, R.;
Radar 97 (Conf. Publ. No. 449) , 14-16 Oct. 1997
Pages:300 - 304

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1 **COHRA: hardware-software cosynthesis of hierarchical heterogeneo distributed embedded systems**
Dave, B.P.; Jha, N.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 17 , Issue: 10 , Oct. 1998
Pages:900 - 919

[Abstract] [PDF Full-Text (504 KB)] IEEE JNL

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2 **COHRA: hardware-software co-synthesis of hierarchical distributed embedded system architectures**
Dave, B.P.; Jha, N.K.;
VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on Jan. 1998
Pages:347 - 354

[Abstract] [PDF Full-Text (1188 KB)] IEEE CNF

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3 **Automatic extraction of functional parallelism from ordinary prograi**
Girkar, M.; Polychronopoulos, C.D.;
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Pages:166 - 178

[Abstract] [PDF Full-Text (1104 KB)] IEEE JNL

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4 **Analysis of several scheduling algorithms under the nano-threads programming model**
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5 **The use of task graphs for modeling complex system behavior**
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Object-Oriented Real-Time Distributed Computing, 1999. (ISORC '99) Proceec
2nd IEEE International Symposium on , 2-5 May 1999
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[Abstract] [PDF Full-Text (92 KB)] IEEE CNF

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6 **Symbolic computing, Lisp languages, and parallel computing**
Furnari, M.M.; Massarotti, A.;
Massively Parallel Computing Systems, 1994., Proceedings of the First Interna
Conference on , 2-6 May 1994
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1 **Task graphs for mobile code-an introduction to ITGS**
Silberman, A.; Stoyen, A.D.;
Object-Oriented Real-Time Dependable Systems, 1999. Proceedings. Fourth International Workshop on , 27-29 Jan. 1999
Pages:239 - 248

[Abstract] [PDF Full-Text (844 KB)] **IEEE CNF**

2 **Heuristic algorithms for scheduling iterative task computations on distributed memory machines**
Tao Yang; Cong Fu;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 8 , Issue: 6 , June 1997
Pages:608 - 622

[Abstract] [PDF Full-Text (508 KB)] **IEEE JNL**